REMARKS

Claims 9-18 are present for reconsideration.

In the **Final Rejection**, claims 9 and 10 were rejected under 35 USC 102(e) as being anticipated by Inaba et al (U.S. Patent No. 6,153,476); claim 11 was rejected under 35 USC 103 as being unpatentable over Inaba et al in view of Naito et al (U.S. Patent No. 5,856,219); and claims 10-18 were rejected under 35 USC 103 as being unpatentable over Inaba et al in view of Naito et al ,as applied against claim 11, and in further view of Moslehi (U.S. Patent No. 5,322,809). It is noted that the Examiner approved the drawing corrections, which were received in the Patent Office on January 28, 2002.

It is respectfully submitted that the rejection of claims 9 and 10 under 35 USC 102 on Inaba et al is in error, since the reference does not teach or suggest the steps being recited in independent claim 9. It is submitted that the Examiner has misinterpreted the teachings of the reference and that the reference does not anticipate or even render obvious the subject matter of independent claim 9. In the rejection, the Examiner has relied on Figs. 5A-5C of the reference to show forming a sacrificial contact in the second region 11a. However, it is submitted that the reference teaches, after forming the structure of Fig. 2B, applying a silicon nitride film (third insulation film) 71 on the entire surface (see column 11, lines 58-62). After the silicon nitride film 71 is formed, a TEOS film 41 for forming the sidewall insulation film 22b is deposited on the entire surface of the resultant structure (see Fig. 5A). Subsequently, an implantation step is carried out to form the impurity diffusion region 25B of a deep junction. During this step, impurity ions are implanted through the silicon nitride film 71 (see Fig. 5B and column 12, lines 14-21).

After the deposition of the interlaying insulating film 31 and subsequent formation of the contact holes 32A and 32B therein, the silicon nitride film 71 remaining in the contact holes 32A and 32B is removed by dry etching or wet etching using hot phosphoric acid (see column 12, lines 33-35). Then, a wiring material is deposited on the interlayer insulating film 31, thereby filling contact holes, such as 32A and 32B. The wiring material is then patterned to form wiring contact portions 33 communicating with the source/drain regions of the MOSFETs 20A and 20B (see column 12, lines 41-49 and Fig. 5C).

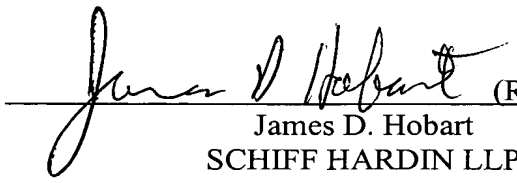
From this, it is completely clear that the silicon nitride film 71 cannot be a sacrificial contact, as used in the semiconductor component according to independent claim 9 of the present application. Silicon nitride is obviously an insulating material and not a conductive material and, therefore, per definition, cannot act as a contact. It is for this obvious reason that the method described in Inaba et al, after the etching of the contact holes 32a and 32b requires the additional etching step to remove the silicon nitride film 71 from the bottom of the contact holes in order to enable the wiring material to contact the respective source/drain regions of the transistor. In fact, Inaba et al refers to silicon nitride film as a third insulation film (see column 11, lines 60-62), which makes it perfectly clear that the silicon nitride film 71 cannot be a sacrificial contact, as used in the integrated semiconductor component according to the present application. It is also noted that nowhere in the reference is the term "sacrificial contact" used. For these reasons, it is respectfully submitted that the subject matter of the method recited in claims 9 and 10 is clearly not anticipated by Inaba et al and would not be obvious in view of the reference.

The secondary references to Naito et al and Moslehi do not supply the missing step which is not taught by Inaba et al. Both of these references are completely silent about providing a sacrificial contact and, thus, do not overcome the deficiencies with the rejection of independent claim 9.

Dependent claims 11-18 are allowable over the combination of Inaba et al with either Naito et al, as applied against claim 11, or in further view of Moslehi, as applied against claims 12 and 18, since the combination does not teach or suggest forming the sacrificial contact, as required and recited in the method of independent claim 9. Thus, while Naito et al may teach a gate electrode material utilizing a polysilicon, and while Moslehi may teach formation of a protective layer 24 having a thickness of 20 to 100nm and removing the layer later to form a silicide on the doped gate path, they do not teach or suggest the fatal defect of the primary reference. Therefore, it is submitted that the dependent claims 11-18 are also unobvious and allowable.

For these reasons, it is respectfully submitted that the rejections of claims 9-18 are in error and should be withdrawn and that the application is in condition for formal allowance. Further reconsideration to that end is earnestly solicited.

Respectfully submitted,



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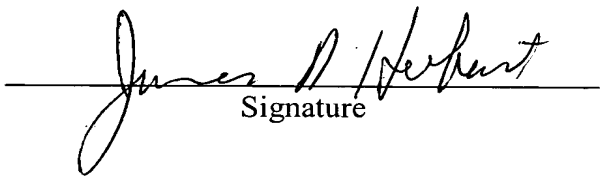

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